1.Yongbo

Fig. 1(a) shows the schematic structure of this hybrid silicon electroabsorption modulator. The lumped electrode configuration gives a very compact design with a footprint of 150m250m, limited primarily by the probe pads that are used here for testing (see Fig. 1(b)). The size can be further reduced if the device is connected to the driving circuits through metal interconnects [9] or microsolder bumps by flip-chip bonding [10]. This device consists of a 100m long effective modulation segment and two 70m multiple-level adiabatic tapers. The cross section of the modulator segment can be found in the photo of Fig. 1(c), which is shot under a tilt angle of 52◦ . It is composed of a silicon ridge and a III-V p-i-n structure. The silicon ridge was defined on a 400 nm thick silicon layer by using a 200 nm-depth dry etch. The III-V structure above the silicon ridge includes a 4m wide, 1.5m high gradually-doped (2e18 to 1e18cm−3) p-InP mesa, a 1.85m wide intrinsic layer, and a thin n-InP extending to the lateral ground metal. The detailed structure of the intrinsic region including the SCH and the MQW is shown in Fig. 1(a) and more information about the epitaxial layers can be found in [7]. The width of the intrinsic region was reduced by an undercut operation through selective wet etching. The undercut process is monitored under a microscope and the control of the etch depth is based on a reference pattern with the target marked on the silicon layer underneath.

The transition tapers between the silicon waveguide and the modulation segment are realized on four different material

layers. As shown in Fig. 1(a), three levels of the taper are defined on the n-InP, MQW/SCH and the p-Mesa, respectively. They are shrunk one layer by one layer with the upper taper tip moving closer to the modulation segment, forming a quasi-vertical taper structure. The taper tips of the n-InP and the p-Mesa are around 400 nm, limited by resolution of the I-line lithography; while the tip width of the MQW/SCH was reduced to less than 100 nm through the wet etching step.

The fourth-level taper is defined on the silicon waveguide (not visible in Fig. 1(a)), with the ridge width reduced from 2m to 1m towards the modulation segment. In order to reduce the device capacitance for high speed operation, the tapers have to be electrically isolated from the main part of the modulator. This is achieved by applying proton implantation to the p-mesa. The 10m long implantation area is located at the end of the taper as shown in Fig. 1(a).

2. XinFu

The III- V layer stack used for the EAM is shown in Table 1. The InAlGaAs multiple-quantum-well (MQW) stack is sandwiched between two separate confinement heterostructure layers (SCHs). It’s composed of 10 compressively strained wells and 11 tensile strained barriers and has its photoluminescence (PL) peak at 1480 nm. Compared with InGaAsP quantum wells, the InAlGaAs quantum wells give a stronger quantum confined stark effect (QCSE) and hence a better modulation efficiency, due to its larger conduction band offset [12]. The layer stack is designed for transverse electric (TE) polarization [13] in the C-band, compatible with conventional semiconductor diode lasers. In our design, the confinement factors in the MQW region and in Si are 0.41 and 0.03, respectively. The superlattice layer structure is incorporated to prevent the propagation of dislocations into the active region due to the bonding.

Figures 2(a) and 2(b) are the cross-sectional view and top view of the EAM, respectively.

The length of the active modulator section is 100 µm and it is 2 µm wide. Benzocyclobutene

(DVS-BCB) is adopted for adhesive bonding and is also used for passivation to decrease the

parasitic capacitance. A lumped electrode structure is adopted, which means the RC time

constant limits the high speed performance of the EAM. The passive silicon waveguide

underneath is a rib waveguide with 1.5 µm width and is 160 nm shallowly etched into the 380

nm silicon layer. The optical coupling between th e silicon device layer and the III-V epitaxial

stack is realized using a bi-level taper consisting of two linearly tapered sections in the III-V

structure. In the first taper section, the opti cal mode is converted from the silicon waveguide

to the MQW (including SCH layers) waveguide without the thick p-cladding layer. Then, the

second taper section adiabatically transforms the waveguide mode to that of the full III-V

structure. The thickness of the Si at the hybrid modulator section is set to be 380 nm to

achieve a better coupling between the Si and III- V waveguides. This is realized by depositing

poly-silicon on the 220nm thick crystalline silicon SOI wafer. We analyze the performance of

the tapers for different values of Lt1, Lt2 and the BCB bonding layer thickness hBCB, using a

commercial software FIMMWAVE [14]. Lt1 and Lt2 are the lengths of MQW taper and p-InP

taper, respectively. Wtip1 and Wtip2 are the widths of the tips of the MQW taper and p-InP

taper, respectively. The BCB thickness is labeled as hBCB. Figures 3(a) and 3(b) show the

coupling efficiency as a function of the lengths Lt1 , Lt2, when hBCB varies. Here we assume

W tip1 = Wtip2 = 0.2 µm, and while one taper is investigated, the other taper is set to be long

enough for adiabatic conversion. From the figures we can find that the smaller hBCB, the better the coupling efficiency and the shorter the tape r length. However, thinner BCB bonding layers

reduce the yield of the bonding process and hence a trade-off needs to be made is selecting the

bonding layer thickness.

In our design, we assume Lt1 = 30 µm, Lt2 = 15 µm and hBCB = 0.03 µm. The mode transformation under this conditio n is presented in Fig. 3(c). The coupling efficiency from the

passive silicon waveguide to the III-V waveguide using this 45 µm long taper can be more

than 95%

Figure 4 shows a schematic diagram of the fabrication process. The silicon photonic components are defined on 200 mm silicon-on-insulator (SOI) wafers with a 380 nm thick poly-silicon / crystalline silicon layer using 193 nm deep UV lithography. The rib silicon waveguides are etched 160 nm deep using inductively-coupled-plasma (ICP) dry etching. The silicon waveguide circuits are then planarized through SiO2 PECVD deposition followed by chemical mechanical polishing down to the silicon device layer. The III-V layer stack is adhesively bonded to this silicon waveguide using a 30 nm thick DVS-BCB layer. The thickness of BCB at different bonding locations may vary by 10% (so 3nm). HCl is then used to remove the InP substrate.

The p-InP mesa with a width of 3.5 μ m is defined by using the top p-metal (Ti/Au) as a

hard mask. The 100 nm InGaAs layer and 1.5 µm InP p-doped layer are etched using selective

wet chemical etching with 1H3PO4: 1H2O 2: 20H2O and 1HCl:1H2O, respectively. The waveguide is oriented along the [0 1-1] direction of the III-V. The width of the p-InP at the bottom is reduced to 2 µm as the orientation of the EAM mesa with respect to the InP crystal

planes introduces an inverted trapezoidal mesa. Afterwards, a 5 µm wide SiN mask is defined

using UV lithography. 20CitricAcid: 1H2O 2 is used for wet etching of the MQW layer and the

MQW is underetched by 3 µm in order to reach 2 µm in width. The etching is selective to the

n-InP beneath. The widths of the tips (Wtip1 = Wtip2 = 0.2 µm) are quite critical for a good

coupling. In this work, such narrow taper tip s are defined using UV lithography and carefully

controlled by wet chemical etching, which demonstrates the manufacturability of these

components in standard III-V processing lines. When the III-V mesa is defined, the n-type

layer is etched using HCl. Then Ni/Ge/Au is deposited for the n-contacts. In the next step, the

III-V structure is encapsulated with DVS- BCB for passivation to decrease parasitic

capacitance. Reactive ion etching (RIE) is used to etch through the DVS-BCB layer to open

the n-contacts and the p-contacts. Finally, ground-signal-ground (GSG) metal contact pads

with 100 μ m pitch are formed for the RF ports. The SEM pictures of the top view and cross section of the EAM are shown in Figs. 5(a) and 5(b), respectively. The inset of Fig. 5(a)

shows the narrow taper tip.

3. Chenzhao

The IIIV/Si hybrid integrated EA modulators/detectors were fabricated using BCB adhesive bonding technology [31], the 3D structure of which is shown in Fig. 2. It includes a 100 µm long and 2 µm wide straight active segment and two 45 µm long bi-level adiabatic tapers for light coupling to and from the passive silicon waveguide [32]. To achieve a better coupling between silicon and IIIV waveguides, a silicon rib waveguide structure constructed with a poly-silicon overlay of 120 nm thickness and 1.5 µm width under the IIIV section is employed [26]. The IIIV layer stack contains InAlGaAs multiple-quantum-wells (MQWs) and two separate confinement heterostructure layers (SCHs) as described in Tab. 1. A picture of the fabricated transceiver chip is shown in Fig. 4. The chip area occupied by one 6-channel transceiver is about 1.5×0.65 mm2, which is mostly taken by the AWGs and the metal contact pads.

4. Me

Fig. 1(a) and 2(b) show the cross-section view and three-dimensional view for the EAM integrated on SOI using BCB adhesive bonding technology [7]. It consists of a silicon ridge waveguide, a thin bonding layer and a III/V p-i-n structure. The silicon ridge waveguide is fabricated on 380nm-thick silicon layer. The thin bonding layer includes around 30nm BCB layer and around 15 nm silica layer. At the top of III/V p-i-n structure, there is a 100nm p-InGaAs layer connected with source metal. Below it, there is a 1.5 μm gradually-doped (2e18 to 1e18 cm-3) p-InP. In the intrinsic region, a multiple-quantum-well (MQW) stack is sandwiched between two In0.52Al0.16Ga0.32As separate confinement heterostructure layers. There are 10 compressive In0.65Al0.09Ga0.26As wells and 11 tensile In0.42Al0.17Ga0.39As barriers composing the MQW. At the bottom of III/V structure, a 150nm thin n-InP layer is connected with ground metal. Detail epitaxial layers parameter is shown in Fig. 2.

The fabrication process of this EAM is similar to that in Referent [1], we simplify the III-V waveguide fabrication using photoresist mask instead of SiN hard mask. The SOI is fabricated through an ePIXfab Multi Project Wafer run. The silicon ridge waveguide is 1.5 μm width and the slab height is 160 nm. The silicon ridge waveguide is planarized with silica. Figure 1(b) show the cross section of the EAM bonded on silicon ridge waveguide. Figure 2(c) show the fabrication results. The upside down trapezoid p-InP mesa with a width of 2.5 µm at top and 1.5 μm width at bottom, by using wet-etching with the photoresist mask. The intrinsic layer is defined by a 5 μm width photoresist mask. By under-etching process, the intrinsic layer is reduced to 1.5 μm width. A 0.1 µm thick Ni/Ge/Au alloy was deposited on n-InP for n-contacts. Then unwanted n-InP is removed away by wet-etching. A 2.5 µm thick DVS-BCB is used for passivation and planarization. The DVS-BCB was etched away in the via-holes for metal connection. A 1 μm thick Ti/Au alloy was deposited on p-InGaAs and n-contacts for 100 μm pitch ground-signal-ground (GSG) metal contact. The top-view photograph for the lump electrode EAM is shown in Fig. 1(d).

Figure 2 (a) also shows the simulated fundamental optical mode for the hybrid silicon waveguide. The optical power confinement in wells is about 24%. The mode conversion from the silicon ridge waveguide to the EAM waveguide is achieved by a 45 µm long bi-level taper. The silicon ridge waveguide keeps straight in the bi-level taper. In the first level, the mode is converted from the silicon ridge waveguide to III-V waveguide without thick p-InP layer, with the intrinsic layer width laterally tapered from 0.2 μm to 1.5 μm. The second level taper transforms the optical mode into the full III-V waveguide mode, with p-InP layer laterally tapered from 0.2 µm to 2.5 µm and the intrinsic layer keeps same. The simulation coupling efficiency between the silicon ridge waveguide and EAM waveguide is about 98%.

EAM with InAlGaAs quantum wells has a strong exciton absorption peak at absorption spectra edge due to its large conduction band offset [12]. Since the band-to-band continuum transition energy, which is above the exciton transition energy, has small influence on the absorption edge, we adopt a theoretical model only contains exciton transition, to simplify calculation the absorption spectra and the shift of absorption edge for the EAM. The material parameters of MQW, such as effective electron/hole mass, Luttinger paramenters, band energy level et. al., are taken from Ref [], according the mole fraction of each element. The half-linewidth for absorption peak varies from 1 meV at zero electric field to 1.4 meV at 42 KV/cm. The effective mass m\*in average matrix element is 0.0064m0, where m0 is the electron mass.

The simulation absorption spectra is shown in figure 3. Due to the p-i-n structure, there is a build-in electric filed in 0 V. The zero electric field in intrinsic is achieved at forward bias 0.6V.

Below 0.6V, the absorption spectra for EAM is calculated based on QCSE. The exciton absorption peak red shifts with applied electric filed increasing. Due to electron-hole overlap integral decrease with electric filed increasing, the absorption magnitude decrease.

Above 0.6V, the absorption spectra for EAM is calculated based on band-filling effect. The exciton absorption peak blue shifts with current injected into conduction band. Due to electron-hole overlap integral keep almost same with current density increased, the absorption doesn’t decrease in magnitude. The exciton transition energy shifts ΔE is given by: ΔE = (1+me/mh)*EF*, where EF is the fermi energy[]. When EF is much higher than lowest conduction subbands E1, EF is linear with carrier density N in quantum well. []. Because the carrier density is proportional to the injected current and the injected current is directly with applied voltage, the absorption peak shifts is directly proportion with applied voltage. In this way, by modulating the applied voltage, we can modulate the output optical power.